CLAIMS

1. A programmable broadband downstream module, comprising:

a bus interface configured to receive a plurality of control data packets and a plurality of transport packets, said plurality of transport packets including:

a plurality of video transport packets communicated asynchronously, a plurality of data transport packets communicated asynchronously, and a plurality of voice transport packets communicated asynchronously;

a programmable CPU operatively coupled to said bus interface, said programmable CPU configured to combine said plurality of transport packets to generate a programmable CPU output; and

a programmable logic operatively coupled to said programmable CPU, said programmable logic configured to generate a synchronous output for said plurality of transport packets.

2. The programmable broadband downstream module of claim 1, further comprising a downstream modulator configured to receive and modulate said synchronous output for downstream transmission, said downstream modulator configured to generate a downstream modulator output.

3. The programmable broadband downstream module of claim 2, further comprising an upconverter operatively coupled to said downstream modulator, said upconverter configured to generate a particular RF frequency output for said downstream modulator output.

4. The programmable broadband downstream module of claim 1, further comprising, a CPU memory support module operatively coupled to said programmable CPU, said CPU memory support module configured to provide memory resources for said plurality of control data packets and said plurality of transport packets.

5. The programmable broadband downstream module of claim 4, further comprising a memory module operatively coupled to said programmable logic, said memory module configured to act as a buffer and store said plurality of transport packets and said plurality of control data packets.

6. The programmable broadband downstream module of claim 1 further comprising an encryption circuit operatively coupled between said programmable logic and said

downstream modulator, said encryption circuit configured to encrypt said synchronous output.

7. The programmable broadband downstream module of claim 1 wherein said plurality of transport packets are a plurality of MPEG-2 transport packets.

8. The programmable broadband downstream module of claim 7 wherein said programmable CPU is configured to perform bit-stuffing.

9. The programmable broadband downstream module of claim 8 wherein said programmable CPU is configured to provide for insertion of control data into said plurality of MPEG-2 transport packets.

10. The programmable broadband downstream module of claim 9 wherein said programmable CPU is configured to perform byte insertions.

11. A programmable broadband downstream module, comprising:

a bus interface configured to receive a plurality of control data packets and a plurality of transport packets, said plurality of transport packets including:

a plurality of video transport packets communicated asynchronously, and a plurality of data transport packets communicated asynchronously;

a programmable CPU operatively coupled to said bus interface, said programmable CPU configured to combine said plurality of transport packets to generate a programmable CPU output; and

a programmable logic operatively coupled to said programmable CPU, said programmable logic configured to generate a synchronous output for said plurality of transport packets.

12. The programmable broadband downstream module of claim 11, further comprising a downstream modulator configured to receive and modulate said synchronous output for downstream transmission, said downstream modulator configured to generate a downstream modulator output.

13. The programmable broadband downstream module of claim 12, further comprising an upconverter operatively coupled to said downstream modulator, said upconverter configured to generate a particular RF frequency output for said downstream modulator output.

14. The programmable broadband downstream module of claim 11, further comprising, a CPU memory support module operatively coupled to said programmable CPU, said CPU memory support module configured to provide memory resources for said plurality of control data packets and said plurality of transport packets.

15. The programmable broadband downstream module of claim 14, further comprising a memory module operatively coupled to said programmable logic, said memory module configured to act as a buffer and store said plurality of transport packets and said plurality of control data packets.

16. The programmable broadband downstream module of claim 11 further comprising an encryption circuit operatively coupled between said programmable logic and said downstream modulator, said encryption circuit configured to encrypt said synchronous output.

17. The programmable broadband downstream module of claim 11 wherein said plurality of transport packets are a plurality of MPEG-2 transport packets.

18. The programmable broadband downstream module of claim 17 wherein said programmable CPU is configured to perform bit-stuffing.

19. The programmable broadband downstream module of claim 18 wherein said programmable CPU is configured to provide for insertion of control data into said plurality of MPEG-2 transport packets.

20. The programmable broadband downstream module of claim 19 wherein said programmable CPU is configured to perform byte insertions.

21. A programmable broadband downstream module, comprising:

a bus interface configured to receive a plurality of control data packets and a plurality of transport packets, said plurality of transport packets including:

a plurality of video transport packets communicated asynchronously, and a plurality of voice transport packets communicated asynchronously;

a programmable CPU operatively coupled to said bus interface, said programmable CPU configured to combine said plurality of transport packets to generate a programmable CPU output; and

a programmable logic operatively coupled to said programmable CPU, said programmable logic configured to generate a synchronous output for said plurality of transport packets.

22. The programmable broadband downstream module of claim 21, further comprising a downstream modulator configured to receive and modulate said synchronous output for downstream transmission, said downstream modulator configured to generate a downstream modulator output.

23. The programmable broadband downstream module of claim 22, further comprising an upconverter operatively coupled to said downstream modulator, said upconverter configured to generate a particular RF frequency output for said downstream modulator output.

24. The programmable broadband downstream module of claim 21, further comprising, a CPU memory support module operatively coupled to said programmable CPU, said CPU memory support module configured to provide memory resources for said plurality of control data packets and said plurality of transport packets.

25. The programmable broadband downstream module of claim 24, further comprising a memory module operatively coupled to said programmable logic, said memory module configured to act as a buffer and store said plurality of transport packets and said plurality of control data packets.

26. The programmable broadband downstream module of claim 21 further comprising an encryption circuit operatively coupled between said programmable logic and said downstream modulator, said encryption circuit configured to encrypt said synchronous output.

27. The programmable broadband downstream module of claim 21 wherein said plurality of transport packets are a plurality of MPEG-2 transport packets.

28. The programmable broadband downstream module of claim 27 wherein said programmable CPU is configured to perform bit-stuffing.

29. The programmable broadband downstream module of claim 28 wherein said programmable CPU is configured to provide for insertion of control data into said plurality of MPEG-2 transport packets.

30. The programmable broadband downstream module of claim 29 wherein said programmable CPU is configured to perform byte insertions.

31. A programmable broadband downstream module, comprising:

a bus interface configured to receive a plurality of control data packets and a plurality of transport packets, said plurality of transport packets including:

a plurality of data transport packets communicated asynchronously, and a plurality of voice transport packets communicated asynchronously;

a programmable CPU operatively coupled to said bus interface, said programmable CPU configured to combine said plurality of transport packets to generate a programmable CPU output; and

a programmable logic operatively coupled to said programmable CPU, said programmable logic configured to generate a synchronous output for said plurality of transport packets.

32. The programmable broadband downstream module of claim 31, further comprising a downstream modulator configured to receive and modulate said synchronous output for downstream transmission, said downstream modulator configured to generate a downstream modulator output.

33. The programmable broadband downstream module of claim 32, further comprising an upconverter operatively coupled to said downstream modulator, said upconverter configured to generate a particular RF frequency output for said downstream modulator output.

34. The programmable broadband downstream module of claim 31, further comprising, a CPU memory support module operatively coupled to said programmable CPU, said CPU memory support module configured to provide memory resources for said plurality of control data packets and said plurality of transport packets.

35. The programmable broadband downstream module of claim 34, further comprising a memory module operatively coupled to said programmable logic, said memory module configured to act as a buffer and store said plurality of transport packets and said plurality of control data packets.

36. The programmable broadband downstream module of claim 31 further comprising an encryption circuit operatively coupled between said programmable logic and said downstream modulator, said encryption circuit configured to encrypt said synchronous output.

37. The programmable broadband downstream module of claim 31 wherein said plurality of transport packets are a plurality of MPEG-2 transport packets.

38. The programmable broadband downstream module of claim 37 wherein said programmable CPU is configured to perform bit-stuffing.

39. The programmable broadband downstream module of claim 38 wherein said programmable CPU is configured to provide for insertion of control data into said plurality of MPEG-2 transport packets.

40. The programmable broadband downstream module of claim 39 wherein said programmable CPU is configured to perform byte insertions.